Chapter 5: The Junction Field Effect Transistor JFET

1. Introduction

A junction field effect transistor, TEC in French and is called JFET in English (Junction Field Effect Transistor). Unlike bipolar transistors whose operation is based on two types of carriers, holes and electrons, unipolar transistors operate with only one type of charge, holes or electrons. They have three electrodes: the source (S), the drain (D) and a control electrode called gate (G).

The operation of the field-effect transistor (FET) can be explained in terms of only majority-carrier (one-polarity) charge flow; the transistor is therefore called unipolar. Two kinds of field-effect devices are widely used: the junction field-effect transistor (JFET) and the metal-oxide-semiconductor field-effect transistor (MOSFET).

2. Partie I : Transistor J-FET

P type substrate (Gate) heavily doped (P +) is deposited: A weakly doped N zone which constitutes the channel, two heavily doped N zones (N +) which constitute input (Source) and output terminals of the channel (Drain). If we reverse the doping we obtain a P-channel field effect transistor.

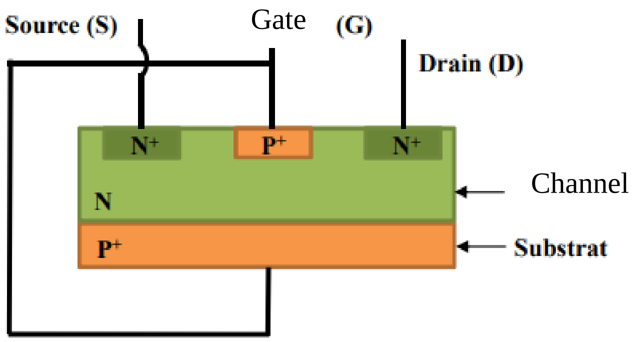


Figure 1 : Structure of N channel JFET transistor

The JFET transistor is made up of three terminals:

1) The source (S) in which injects the carriers of charges into the structure.

2) The drain (D) in which collects the carriers: the drain.

3) The Gate (G) where the control voltage is applied.

2.1. JFET construction and symbols

Conduction is ensured by the passage of charge carriers from source (S) to drain (D) through the channel between the gate (G) elements.

The transistor can be an N-channel device (conduction by electrons) or an P-channel device (conduction by holes);

The following figures illustrate the basic structure of a JFET transistor.

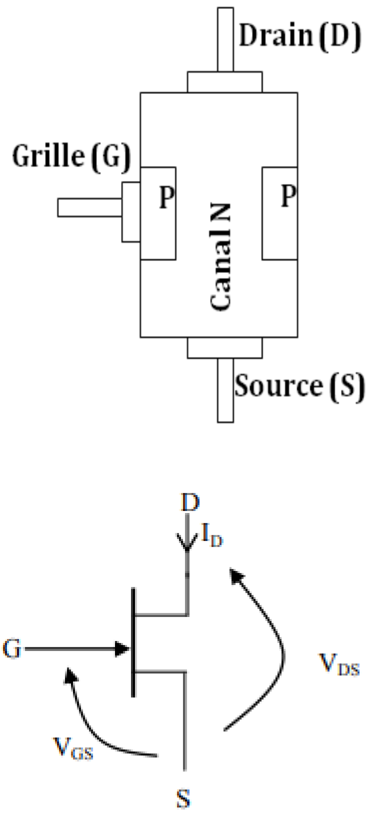


Figure 2 : N channel JFET

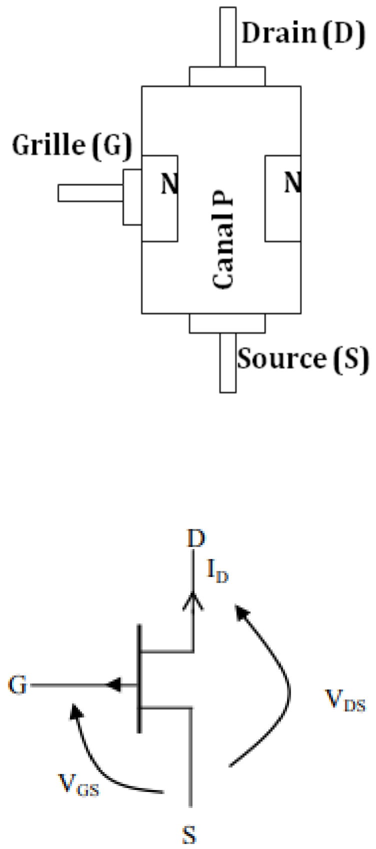


Figure 3 : P channel JFET

- ✓ If we put an FET under a VGS voltage, we expand or narrow the channel allowing the circulation of carries between the drain and the source.
- ✓ We speak of an N channel when the doping of this channel is of type N, and of a P channel in the opposite case.
- ✓ Depending on the type of channel, the VGS sign allows to modify its size.

2.2. Voltages and currents

The JFET transistor has three terminals, three currents and three voltages must be defined:

For an N-channel JFET in normal operation:

1) The VDS voltage is positive

2) The VGS voltage is negative or weakly positive (< 0.6 V)

3) The gate current is almost zero IG = 0. Law of nodes: IS = ID

4) Current enters the transistor through the drain (ID)

5) The current leaves the transistor through the source (IS)

2.3. Fonctioning fo N-Channel JFET

The N-channel field effect transistor is controlled by applying a Gate Source voltage VGS:

- Negative VGS in the case of an N type, and the drain is positively polarized with respect to the source. Positive VGS in the case of type P.
- The drain-source space receives a bias voltage (VDS voltage)

The JFET conducts if VGS≥VP, VP is the pinch-off voltage (closed channel, ID=0), it is a negative reverse voltage.

3. The characteristics of N-channel JFET

In this section we will deal with the characteristics of a JFET transistor:

3.1. Output characteristic ID=f(VDS) with VGS constant

When we set for example VGS=0, the channel N behaves like a resistor RD and we see that the drain current ID increases with the drain source voltage VDS in a practically linear manner up to a value equal to VP (pinch voltage).

From this voltage (pinch voltage) the current ID no longer varies and keeps a practically constant value equal to IDSS (max current for a JFET). In this case we say that the saturation range has been reached.

Note: It should be noted that the VDS voltage cannot increase indefinitely without the risk of destroying the transistor. We therefore limit VDS to a maximum voltage which we note VDS max.

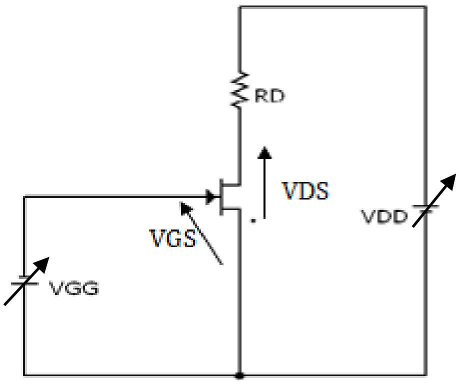


Figure 4 : N channel JFET Biasing circuit

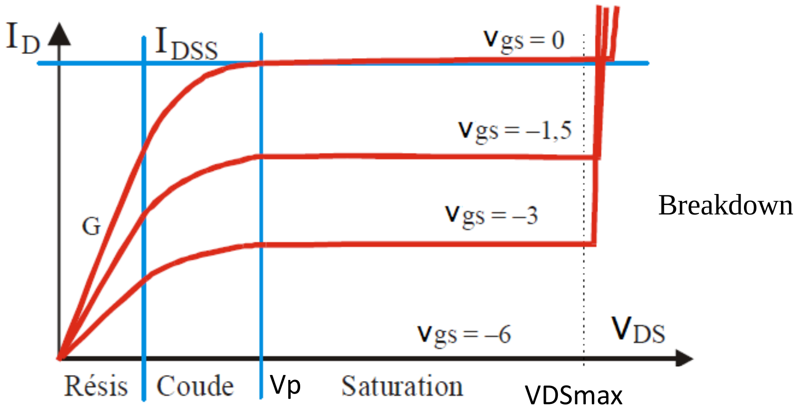


Figure 5 : Output characteristic ID=f(VDS)

- The active region of the JFET is located between voltages VP and VDSmax.
- Vp: pinch voltage (closed channel ID=0 for VGS=VP). VP is the value of VDS for which the drain current becomes constant and is always measured when VGS=0
- VGSoff and VP are always equal but in opposite sign
- IDSS represents the current between the drain and the source when the gate is connected to the source (short-circuited gate); This is the maximum current that an JFET can produce.

The Figure above defines the four working areas of a JFET:

1. The Ohmic region: When VDS is very small, the JFET functions as a controlled resistor.

2. The active or saturation region:

- It is in this area that we will use the FET.
- The JFET acts as a current source controlled by the gate voltage.

3. The breakdown region: The voltage VDS between the drain and the source is high enough to create a breakdown of the resistive channel. The current ID then increases in an uncontrolled manner.

3.2. Transfer characteristic ID=f(VGS) with VDS constant

The evolution of the drain current ID as a function of VGS with VDS =Cste is represented by Figure 6.

The defining equation of this curve is given by:

$$ID = IDSS[1 - \frac{VGS}{VGSoff}]^2$$

IDSS : Drain Source current for VGS=0.

$$VGSoff = -Vp$$

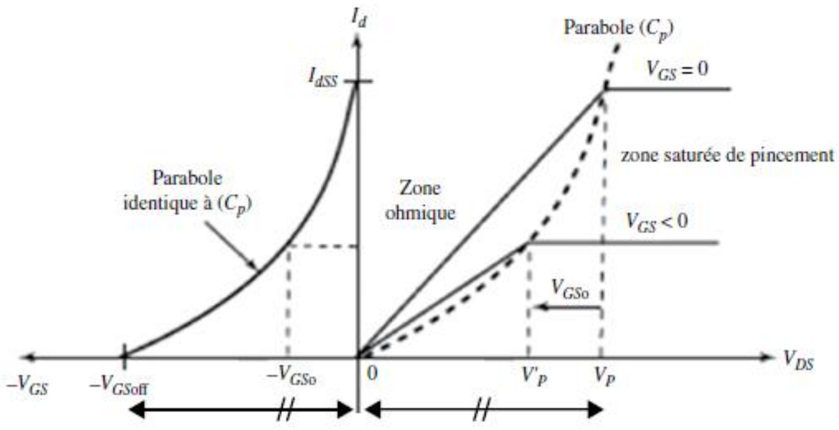


Figure 6 : Transfer characteristic $ID = f(VGS)$

From the curve ID=f(VGS), we define what we call the slope or the transconductance gm (AC) of a field effect transistor.

$$gm = \frac{\Delta ID}{\Delta VGS} = \frac{dID}{dVGS}$$

$gm = gm0(1 - \frac{\text{VGS}}{\text{VGSoff}})$ with

gm0=-2IDSS/VGSoff

gm0 : Transconductance at VGS=0

3. Static study of a JFET transistor

3.1. Static load line and rest point

1) The static load line is expressed by: ID=f(VDS).

2) The operating point defined by the point of intersection between the static load line and the characteristic.

3) The operating point (rest) is fixed by an ordinate IDQ, and an abscissa VDSQ.

3.2. Bias circuits of a JFET transistor

In the same way as for the bipolar transistor we must choose an operating point before defining the small signal parameters because these will be a function of this operating point. To do this, the transistor must be polarized.

3.2.1. Automatic biasing

In the case of automatic polarization, only one source is applied (VDD) as shown in the figure below:

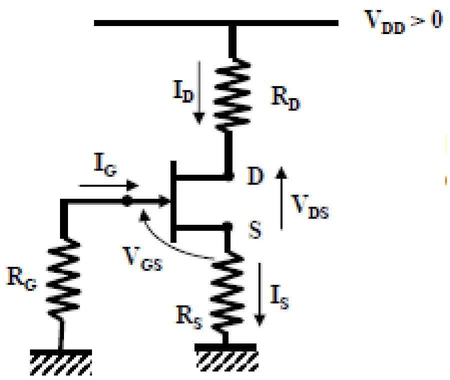


Figure 7 : Automatique polarisation of JFET

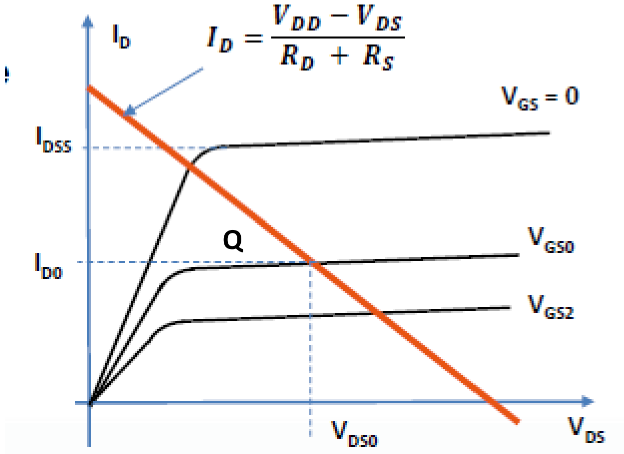
Required work: write the equation of the load line.

- load Line eqaution:

$VDD - VDS = RD\ ID - Rs\ ID$

$IS = ID \Longrightarrow ID = (VDD - VDS)/(RS + RD)$

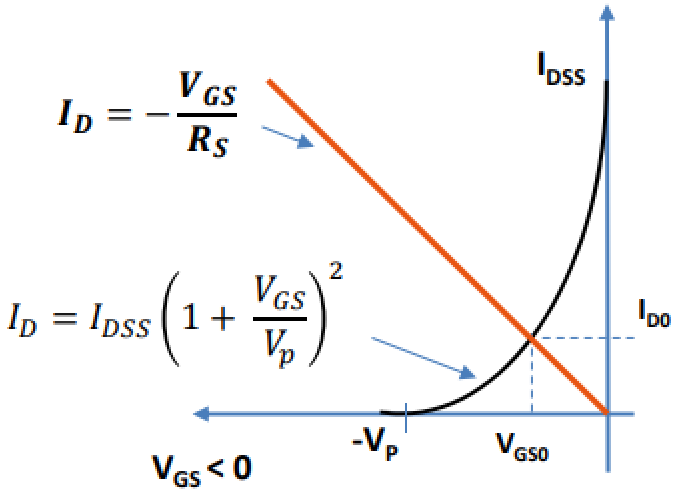
The operating point is described by the point Q, and shown schematically on the graph.



- Attack line equation :

$VGS = -RGIG - RSIS$ (IG≈ 0) ⇒

$ID = -VGS/RS$



3.2.1. Biasing by two independent sources

In this type of polarization two voltage generators are applied; one at the grid and the other at the Drain terminal.

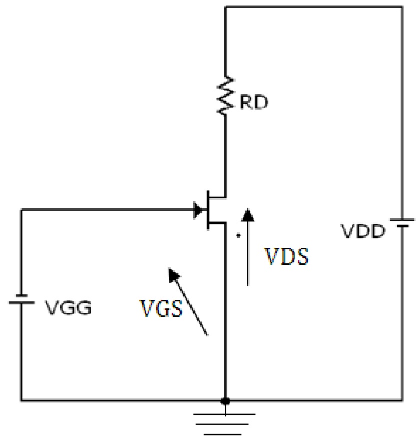


Figure 8 : Biasing of a JFET by two independent sources

The load line can be written as follow:

$ID = (VDD - VDS)/RD$

3.2.2. Biasing with a single voltage source

In this type of polarization a single source is applied at the gate and the drain.

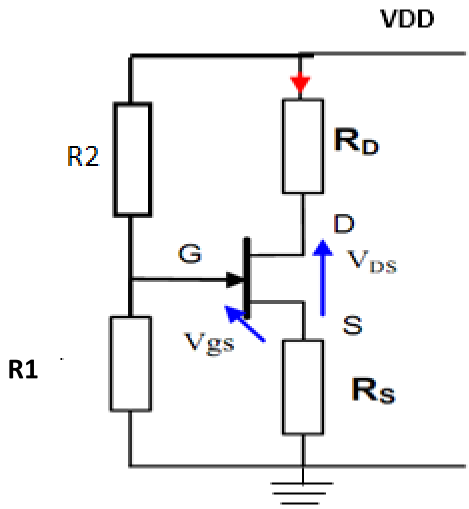


Figure 9 : Polarisation d'un JFET

The load line can be written as follow : $ID = (VDD - VDS)/(RD + RS)$

4. Equivalent diagram of a small signal JFET at low frequency

The equivalent diagram of the JFET in a small signal regime and at low frequency is given in the following figure:

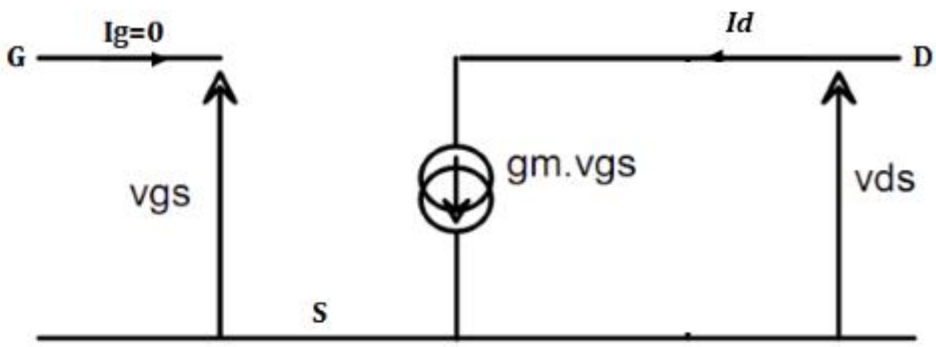


Figure 10 : Low frequency equivalent model of a JFET

gm : the transconductance of the transistor, is the slope of the transfer characteristic ID (VGS).

The exploitation of the equivalent diagram of the transistor will make it possible to calculate the following quantities:

- Voltage amplification $A_v = \frac{v_2}{v_1}$
- Input Impedance $Z_e = \frac{v_1}{i_1}$
- Output Impedance $Z_s = \frac{v_2}{i_2}$

Note :

In the dynamic regime:

- ✓ The capacitors C are replaced by short circuits at the signal frequency.
- ✓ The DC voltage source is replaced by earthing.

5.3. Amplificateurs à FET à faible signaux

Comme pour le transistor bipolaire, il existe trois montages types pour le TEC. L'étude des performances de ces montages se fait par l'évaluation du gain en tension, et des impédances d'entrée et de sortie.

5.3. Low-signal FET amplifiers

As with the bipolar transistor, there are three typical configurations for the JFET transistor. The performance of these circuits is studied by evaluating the voltage gain, and the input and output impedances.

5.3.1. Common Source FET Amplifier

We consider the study the common source FET amplifier given in the figure below:

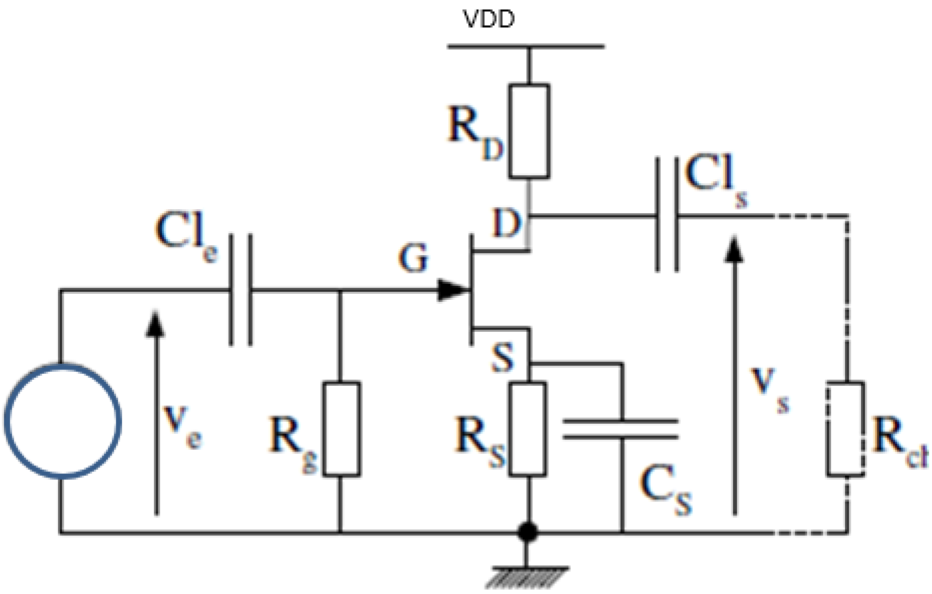
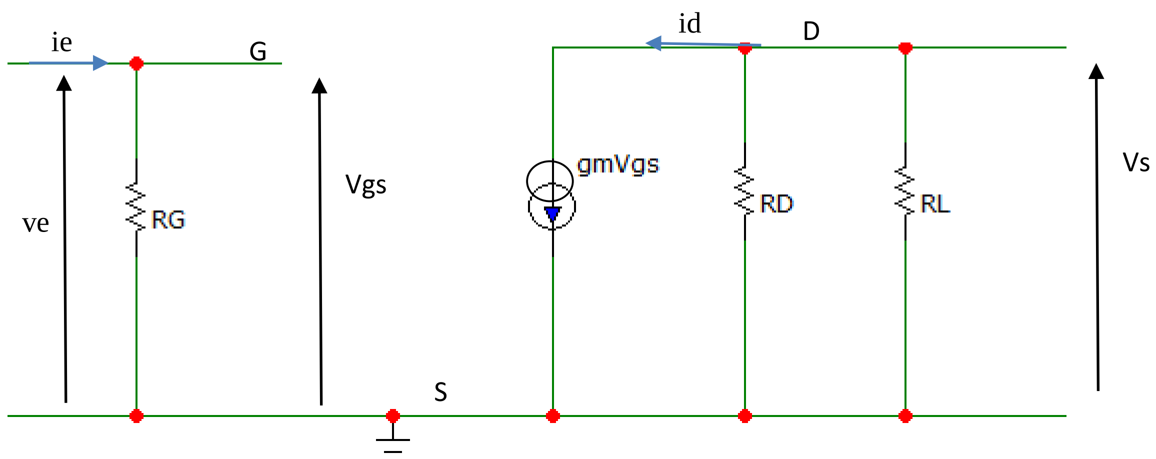


Figure 11 :Common source FET

Work required: Calculate Av, Ze and Zs.

1) **Dynamic study**



2) Voltage Amplification **Av= ?**

we pose : $Rd = RD//RL$

$id = gmVgs$ (1)

$ve = vgs$ (2)

$vs = -rd.id$ (3)

We replace equation (1) in equation (3) ⟹Vs=-$rd.gm.Vgs$

(4)

$\frac{4}{1}$ gives $Av = -rd.gm$

3) Input impedance $Re = \frac{Ve}{ie}$

$Ve = Rg.ie \Longrightarrow \frac{Ve}{ie} = Rg$

4) Output impedance $Rs = ?$

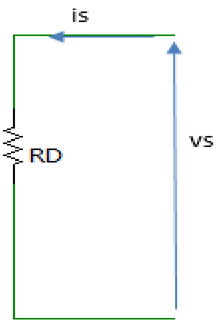
For that it is necessary :

- Remove the RL load

- Cancel input generator eg (DC all voltage sources)

Apply a voltage generator instead of RL

Calculate Zs=Vs/is



$$Rs = \frac{Vs}{is} = \mathrm{RD}$$

5.3.2. Common Drain FET Amplifier

We consider the following common drain FET amplifier:

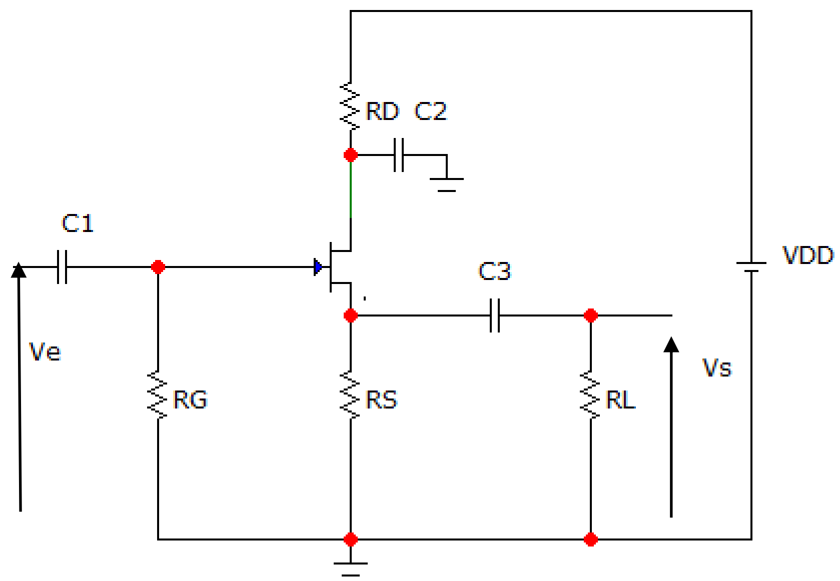
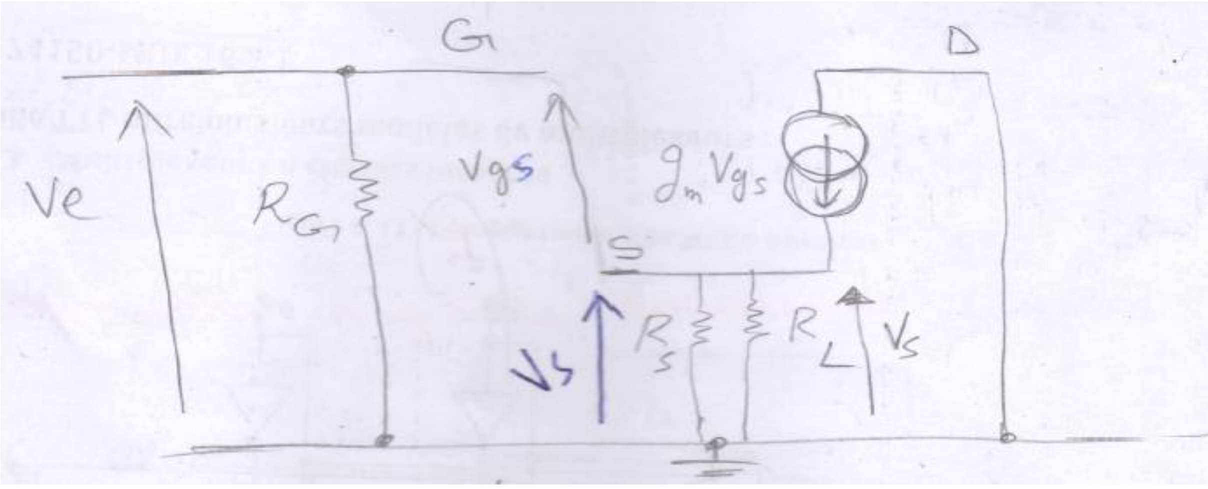


Figure 12 : Common drain FET

Work : Calculate Av, Ze et Zs.

1) The equivalent alternative diagram is given in the figure bellow :



Required work : Calculate Av, Re et Rs.

1) Volatge gain $A_v = \frac{V_s}{V_e}$

We pose : $r_s = R_s \,//\, R_L$

$V_e = V_{gs} + V_s$ (1)

$V_s = r_S g_m V_{gs}$ (2)

We replace equation (2) in equation (1), we obtain :

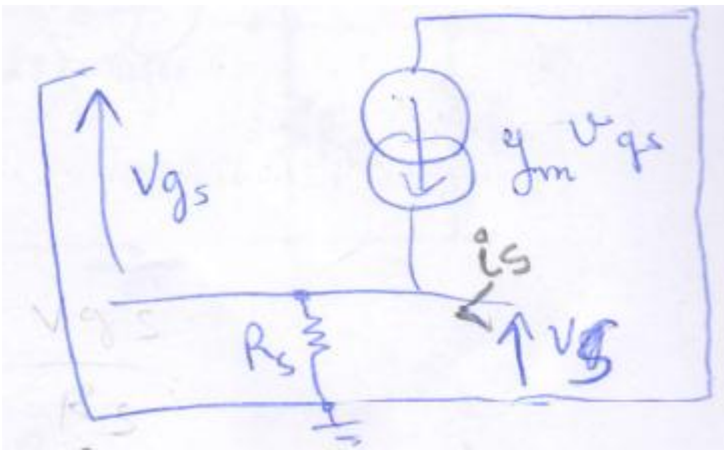
$V_e = V_{gs}(1 + r_S g_m)$ (3)

(2)/(3) give : $A_v = \frac{g_m r_s}{1+r_S g_m}$

2) Input impedance $R_e = \frac{V_e}{i_e}$

$R_e = R_G$

3) Output impedance $Rs = \frac{vs}{is}$



$V_s = (is + gm.vgs)Rs$ (4)
$V_s = -V_{gs}$ (5)

We replace equation (5) in equation (4), we obtain :

$$i_s - g_m V_s - \frac{V_s}{R_s} = 0 \;\Rightarrow\; i_s = v_s\left(g_m + \frac{1}{R_s}\right)$$

➔$R_s = \frac{1}{g_m + \frac{1}{R_s}}$

5.3.3. Common Gate FET Amplifier

Consider the following common gate FET amplifier:

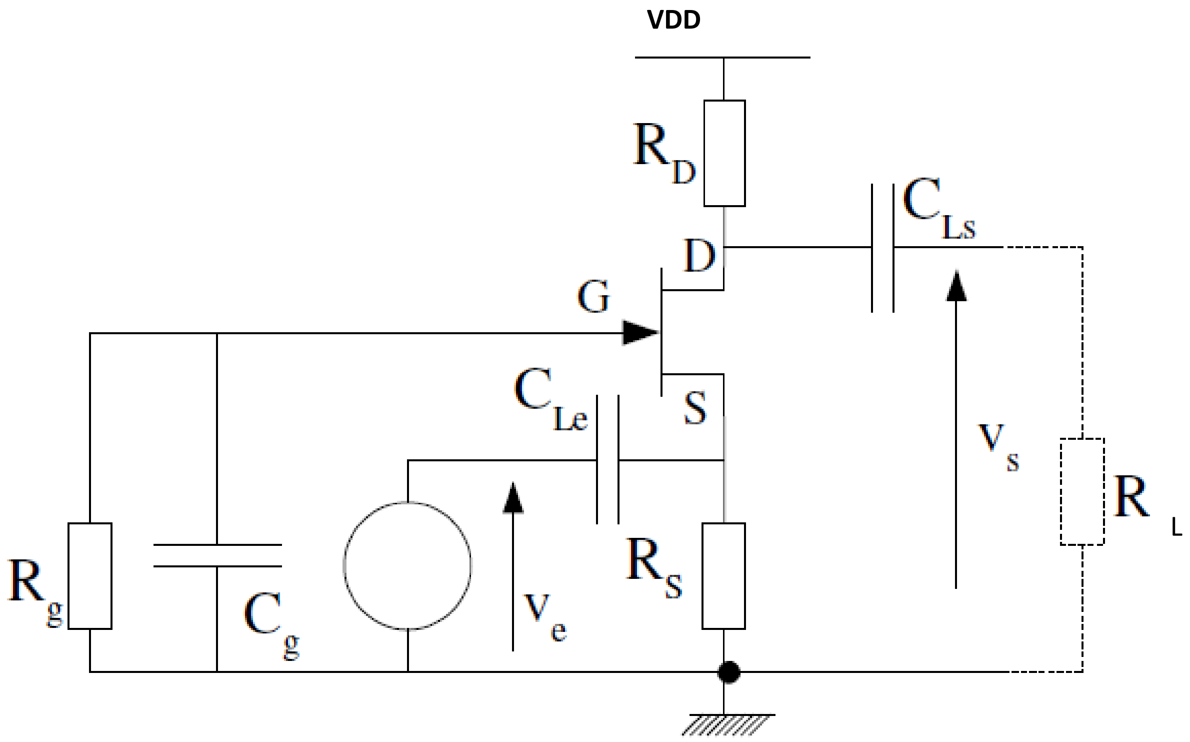
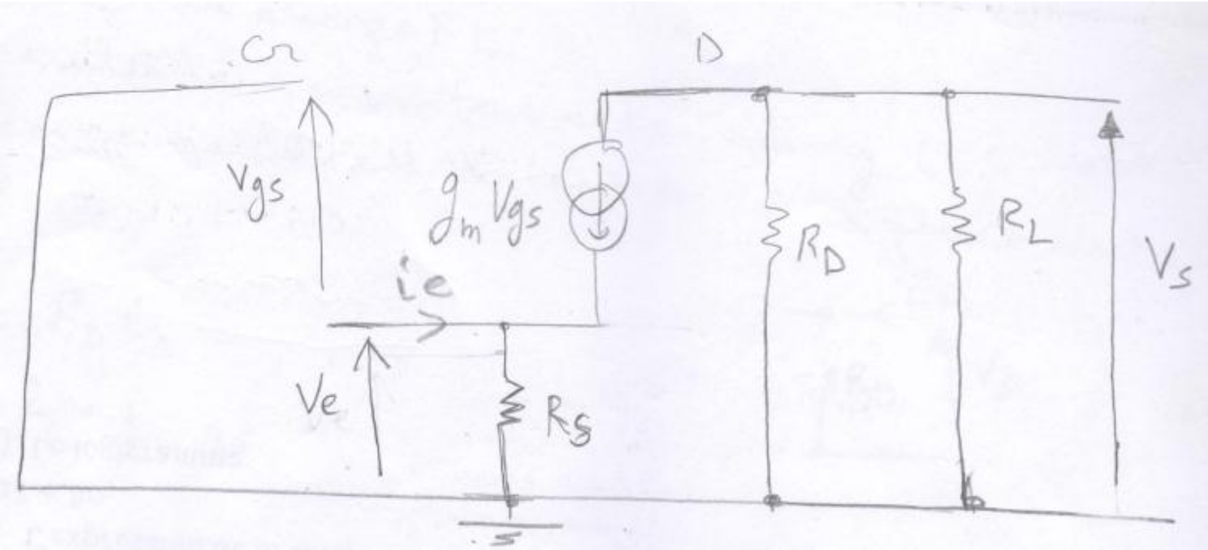


Figure 13 : Common Gate FET Amplifier

Required work : Calculate Av, Ze et Zs.

1. Equivalent scheme of the common gate FET in dynamics



We have: $V_s = -V_{gs}$

1) Voltage amplification

we pose : $r_d = R_D // R_L$

we have :

$v_e = -v_{gs}$ (1)

$V_s = -r_d g_m V_{gs}$ (2)

Eqaution 1/equation 2, on obtient : $\frac{V_s}{V_e} = \frac{V_s}{V_{gs}} = r_d g_m$

$A_V = g_m r_d$

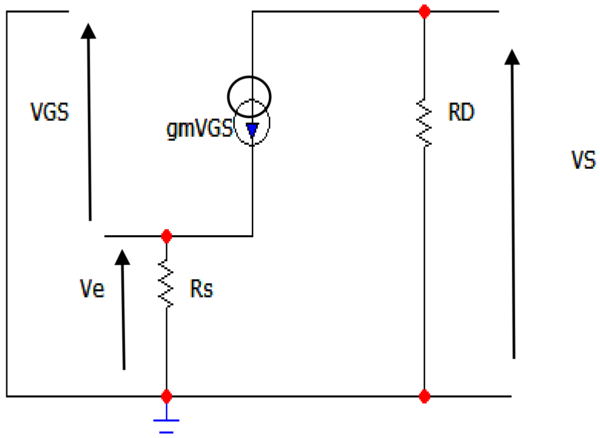
1) Input impedance $R_e = \frac{V_e}{i_e}$

$V_e = R_s(i_e + g_m V_{gs})$

$V_e = -V_{gs}$

$$i_e + V_{gs}\left(g_m + \frac{1}{R_s}\right) = 0$$

$i_e = -V_{gs}\left(g_m + \frac{1}{R_s}\right) \rightarrow R_e = \frac{V_e}{i_e} = \frac{1}{g_m + \frac{1}{R_s}}$



2) Output impedance

- Disconect the load R_L
- Cancel the voltage generator eg (we short-circuit the voltage sources)
- Place the voltage generator in the place of R_L

$vgs = 0 \Rightarrow gmvgs = 0$

$V_s = R_D i_s \Rightarrow R_s = \frac{v_s}{is} = R_D$